08/971,499 (the" '499 Application") which matured into the '353 Patent, Applicant respectfully submits that it is not barred from seeking the issuance of apparatus claims via the present reissue patent application. See Scripps Clinic & Research Foundation v. Genentech, Inc., 18 U.S.P.Q. 2d 1001 (Fed. Cir. 1991).

New independent Claim 7 is directed to a chip stack comprising at least two packaged chips which are described as each having opposite sides and a multiplicity of leads extending from each of the opposite sides thereof. As further recited in Claim 7, the chip stack also includes at least one frame which is described as extending along at least each of the opposite sides of the packaged chips. The frame is further described as comprising an upper surface having only first and second rows of conductive pads disposed thereon and extending along respective ones of the opposite sides of the packaged chips, and a lower surface having only third and fourth rows of conductive pads disposed thereon which also extend along respective ones of the opposite sides of the packaged chips. In Claim 7, the leads of one of the packaged chips are described as being electrically connected to respective ones of the conductive pads of the first and second rows disposed on the upper surface of the frame, with the leads of the other packaged chip being described as electrically connected to respective ones of the conductive pads of the third and fourth rows disposed on the lower surface of the frame.

New Claim 8 is dependent upon Claim 7 and describes the packaged chips as each comprising a TSOP packaged chip. Finally, new Claim 9 is also dependent upon Claim 7 and describes the conductive pads of the first and second rows disposed on the upper surface of the frame as being electrically connected to respective ones of the conductive pads of the third and fourth rows disposed on the lower surface of the frame.

Applicant respectfully submits that the antecedent basis for the various limitations recited in new Claims 7-10 in the specification of the '353 Patent is as follows:

1. Claim 7 - column 4, lines 8-20; column 4, lines 39-59; column 6, lines 6-9; column 6, lines 40-44; and column 7, lines 50-60.

2. Claim 8 - column 4, lines 20-27.

3. Claim 9 - column 4, lines 59-65; and column 6, lines 9-16.

Applicant respectfully submits that its prior U.S. Patent No. 5,612,570 (the " '570 Patent") referred to in the specification of the '353 Patent and cited as the primary reference in support of an obviousness rejection during the prosecution of the '499 Application does not teach, suggest or show a chip stack apparatus as recited in new independent Claim 7. The '570 Patent is directed to a chip stack comprised of a stack of chip packages mounted on a substrate. Each of the chip packages includes a packaged chip which is mounted within a central aperture of a frame and electrically interconnected to conductive pads on the frame. More particularly, the leads extending from opposite ends of the plastic package of the packaged chip are soldered to the conductive pads which are disposed on the upper surface of the frame on opposite sides of the central aperture defined thereby. Conductive traces on the opposite upper and lower surfaces of the frame combine with vias extending through the frame to couple or electrically connect the conductive pads to which the leads of the plastic package of the packaged chip are soldered to other groups of conductive pads disposed on the upper and lower surfaces of the frame adjacent the outer edges thereof.

With particular reference to Figures 5, 8 and 10 of the '570 Patent, disposed on the upper surface 24 of the frame 26 adjacent opposite ends 28, 30 of the central aperture 32 are rows of conductive pads 20, 22. Some of the conductive pads 20, 22 are electrically connected via conductive

traces 48 to respective ones of a plurality of conductive pads 34 which are also disposed on the upper surface 24 of the frame 26 adjacent the outer edges thereof. The traces 48 are also used to electrically connect selected ones of the conductive pads 20, 22 to respective ones of a plurality of vias 50 which extend through the frame 26 and are electrically connected via conductive traces 52 to respective ones of a plurality of conductive pads 38 which are disposed on the lower surface 36 of the frame 26 adjacent the outer edges thereof. The leads 18 extending from opposite ends of the package 16 are soldered to only the conductive pads 20, 22 disposed on the upper surface 24.

In the chip stack recited in new independent Claim 7, the upper surface of the frame is described as having only two rows of conductive pads thereon. Similarly, the lower surface of the frame is described as having only two rows of conductive pads thereon. The electrical connection of the leads of the packaged chips to the conductive pads on the upper and lower surfaces of the frame in the chip stack recited in Claim 7 is accomplished without the use of the conductive pads 34, 38 and conductive traces 48, 52 described in the '570 Patent.

As is evident from the specification of the '353 Patent, the electrical connection of the leads 16 of the packaged chips 14 to the conductive pads 26 is accomplished by the electrical connection of the leads 16 directly to the conductive pads 26 on the upper and lower surfaces of the frame 22, and the electrical connection of the conductive pads 26 on the upper surface of the frame 22 directly to respective ones of the conductive pads 26 on the lower surface thereof which is accomplished without the use of conductive traces. In this respect, in contrast to the frame 26 described in the '570 Patent which includes four rows of conductive pads on the upper surface 24 thereof (i.e., the conductive pads 20, 22, 34), the conductive traces 48 on the upper surface 24 thereof, and the conductive traces 52 on the lower surface 36 thereof, the frame of the chip stack recited in Claim 7

is significantly more simple in structure due to its inclusion of only two rows of conductive pads on the upper surface of the frame and absence of any conductive traces. Because the leads of the packaged chips are electrically connected directly to respective ones of the conductive pads of the two rows disposed on each of the upper and lower surfaces of the frame which are themselves electrically connected to each other without the use of conductive traces, the chip stack recited in Claim 7 is more simple in design and thus easier to manufacture at a significantly reduced cost as compared to the chip stack described in the '570 Patent.

On the basis of the foregoing, Applicant respectfully submits that new Claims 7-10 are in condition for allowance.

Respectfully submitted,

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